

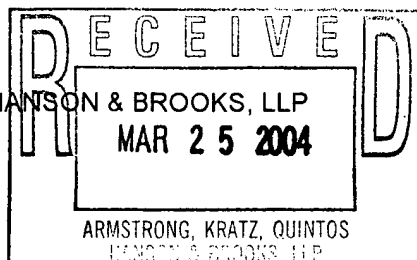
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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/735,886	12/16/2003	2811	770	031325	28	18	3

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ARMSTRONG, KRATZ, QUINTOS, HANSON & BROOKS, LLP
1725 K STREET, NW
SUITE 1000
WASHINGTON, DC 20006



CONFIRMATION NO. 5693

FILING RECEIPT



OC000000012172433

Date Mailed: 03/24/2004

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

Toshio Takayama, Kawasaki, JAPAN;
Kuniyuki Narukawa, Kasugai, JAPAN;
Hiroshi Mizutani, Kasugai, JAPAN; --Hirashi--

Assignment For Published Patent Application

FUJITSU LIMITED, Kawasaki, JAPAN;

Domestic Priority data as claimed by applicant

Foreign Applications

JAPAN 2002-371134 12/20/2002

If Required, Foreign Filing License Granted: 03/23/2004

Projected Publication Date: 07/01/2004

Non-Publication Request: No

Early Publication Request: No

Title

DOCKETED

DATE

Semiconductor device having a multilayer interconnection structure and fabrication process thereof

Preliminary Class

257

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Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **TAKAYAMA, Toshio, et al.**

Attention: **Applications Division**

Serial Number: **10/735,886**

Group Art Unit: **2811**

Filed: **December 16, 2003**

P.T.O. Confirmation No.: 5693

For: **SEMICONDUCTOR DEVICE HAVING A MULTILAYER
INTERCONNECTION STRUCTURE AND FABRICATION PROCESS
THEREOF**

REQUEST FOR CORRECTED FILING RECEIPT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Date: April 7, 2004

Sir:

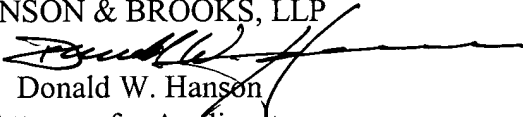
Please supply the undersigned attorney with a corrected filing receipt for the above-identified application. The undersigned also respectfully requests that the Patent and Trademark Office records be amended to reflect the correction.

In reviewing the official Filing Receipt, we noted an error in that the **third assignee's name is misspelled and should read as - HIROSHI, MIZUTANI- .** A copy of the **Declaration** is enclosed which indicates the correct information. We are enclosing a copy of the filing receipt with the corrections highlighted.

In the event that any fees are required in connection with this paper, please charge our Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, KRATZ, QUINTOS,
HANSON & BROOKS, LLP


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Enclosures: Official Filing Receipt; and Declaration